

# MS-7437 (MS-6632,MS-6633,MS-6639)

Version 1.0

## CPU:

Intel Dimondville

## System Chipset:

Intel 945GSE (North Bridge)

Intel ICH7M(South Bridge)

## On Board Chipset:

Clock Generator - ICS9LPRS113

HD AUDIO CODEC(ALC888)

Giga LAN -- Realtek RTL8111C

LVDS CHRONTEL - CH7308B

SIO-Fintek F71882F

Card Reader RTS5158E

AMP - TPA3005D2

BIOS -- SPI

## Main Memory:

DDR II SO-DIMM x 1 (Max 1GB)

## Expansion Slots:

Internal Mini PCIE 1

Internal Mini PCIE 2 (Option)

CF Card Connector

## Intersil PWM:

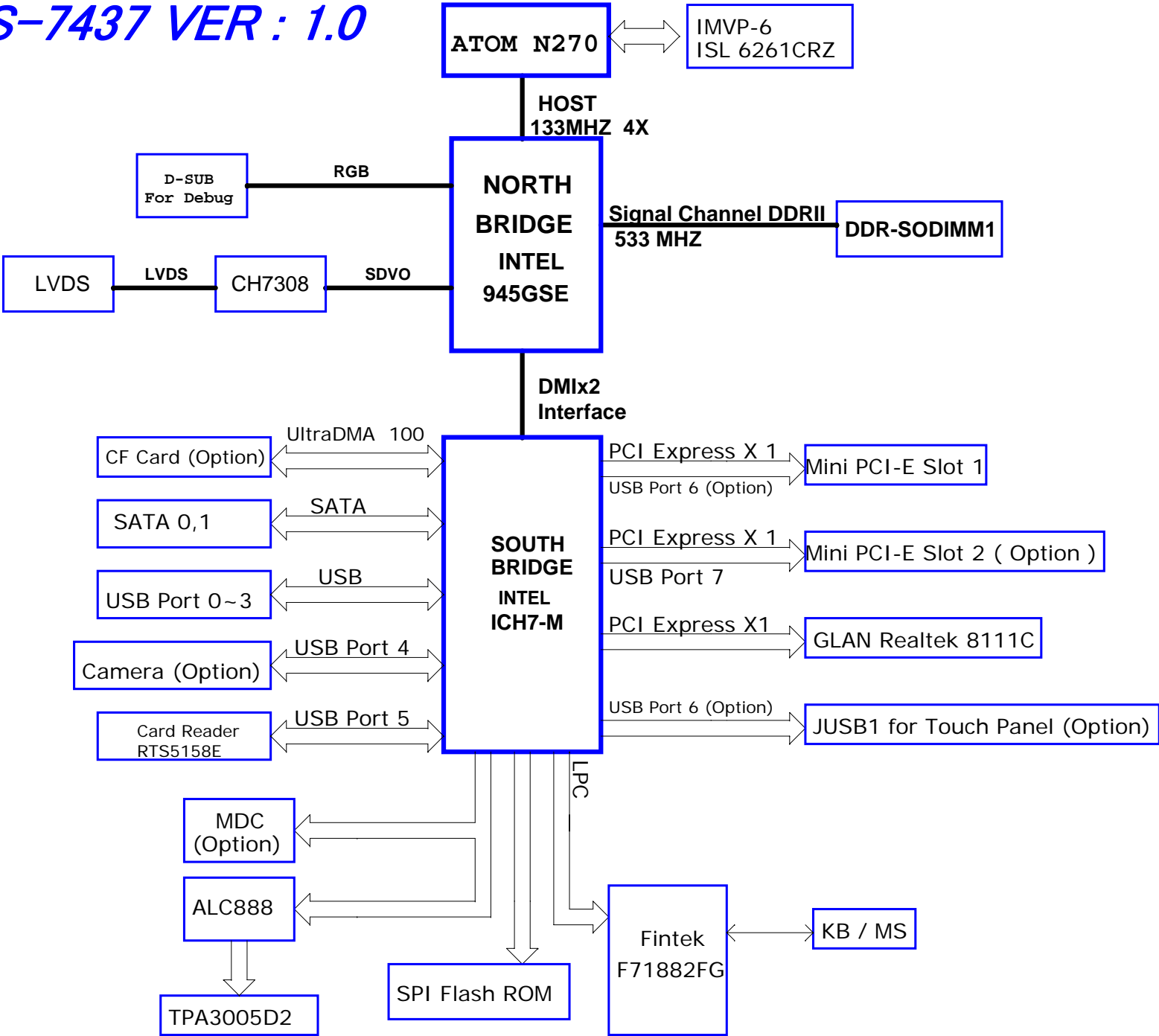
Controller: ISL6261CRZ-T

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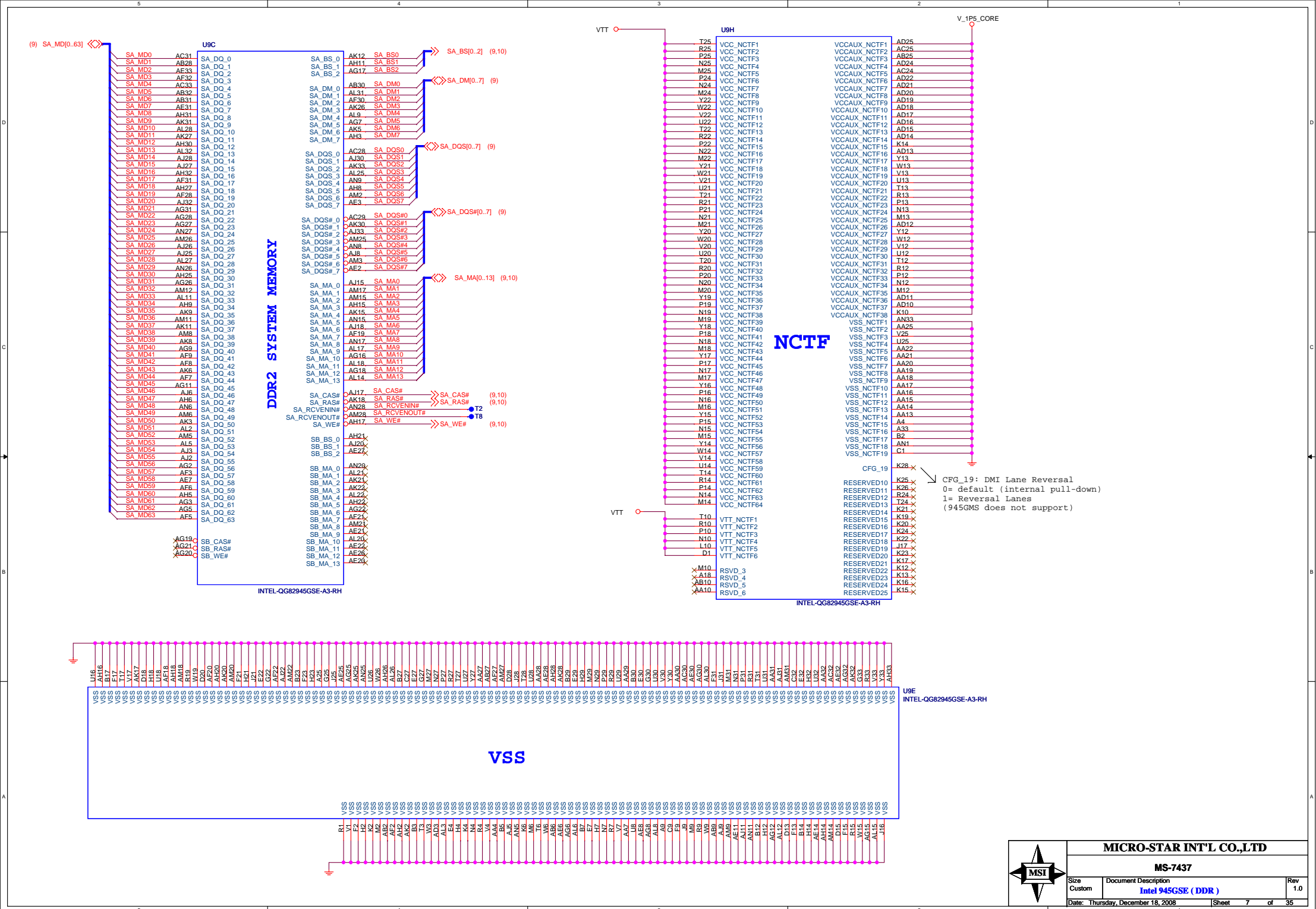












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**Intel 945GSE ( DDR )**

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# 945 GSE Power

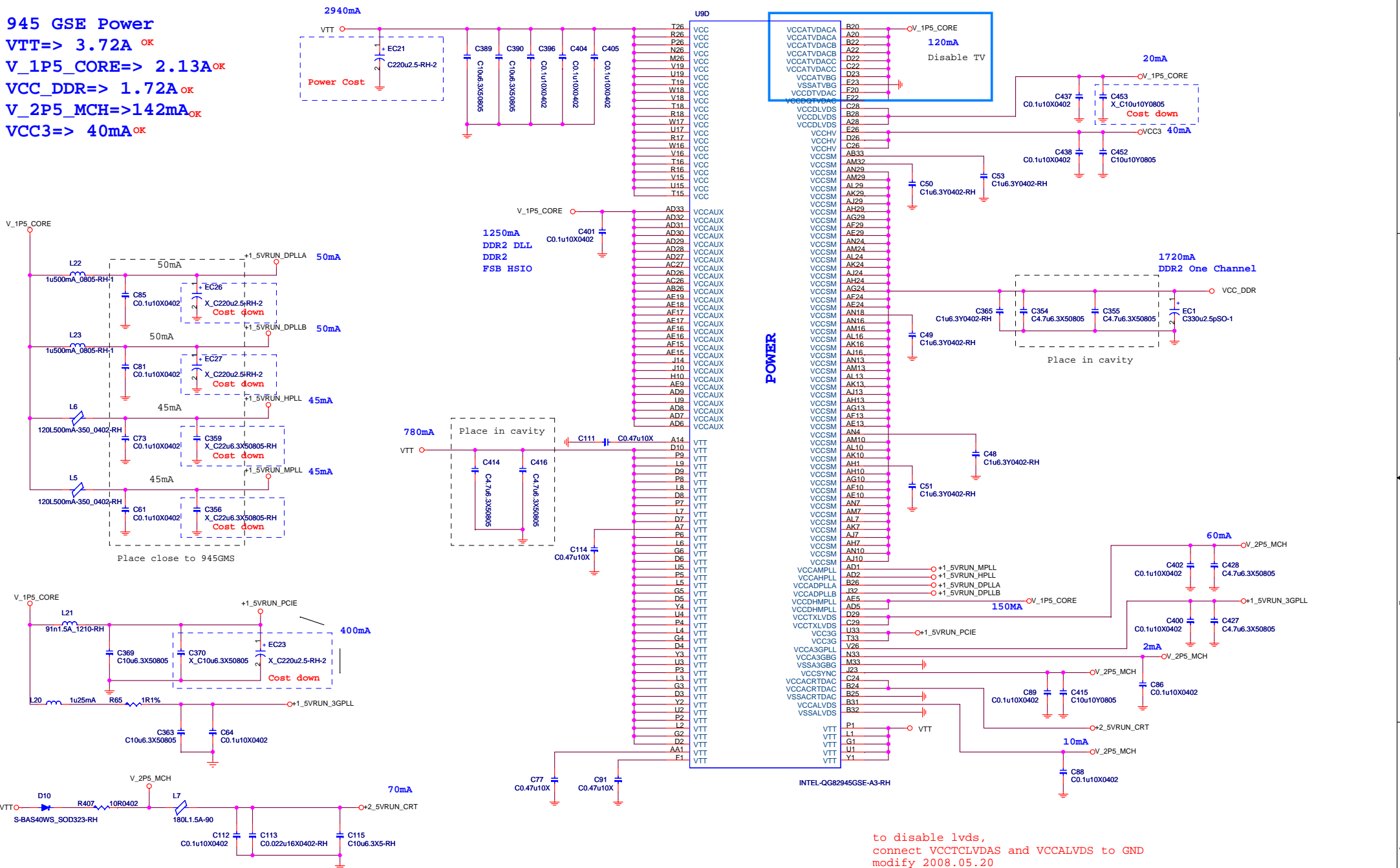
VTT=> 3.72A OK

V\_1P5\_CORE=> 2.13A OK

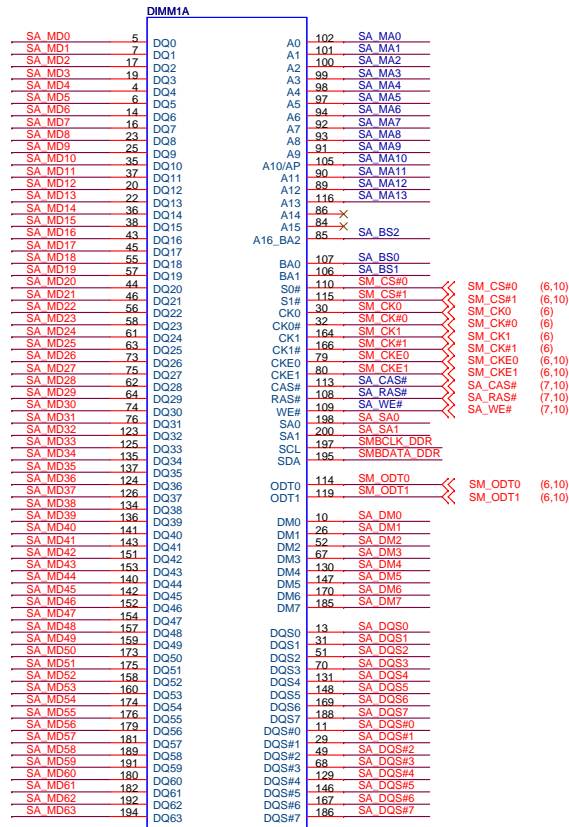
VCC\_DDR=> 1.72A OK

V\_2P5\_MCH=>142mA OK

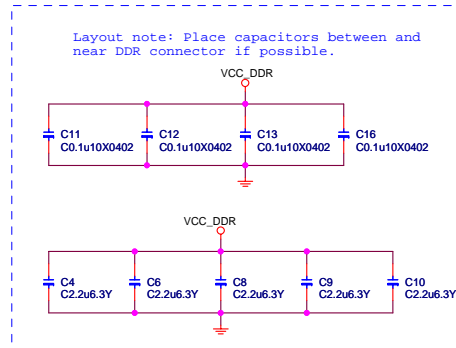
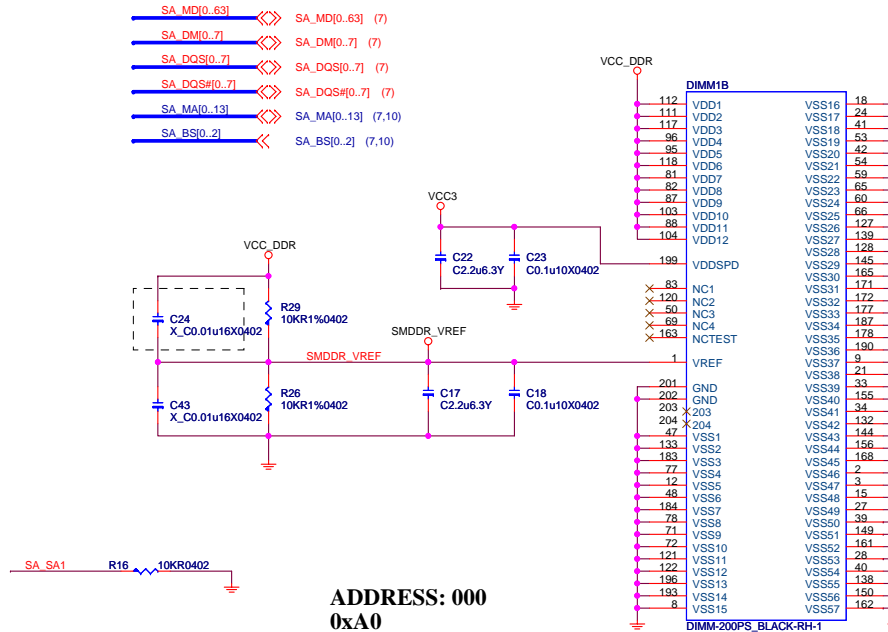
VCC3=> 40mA OK

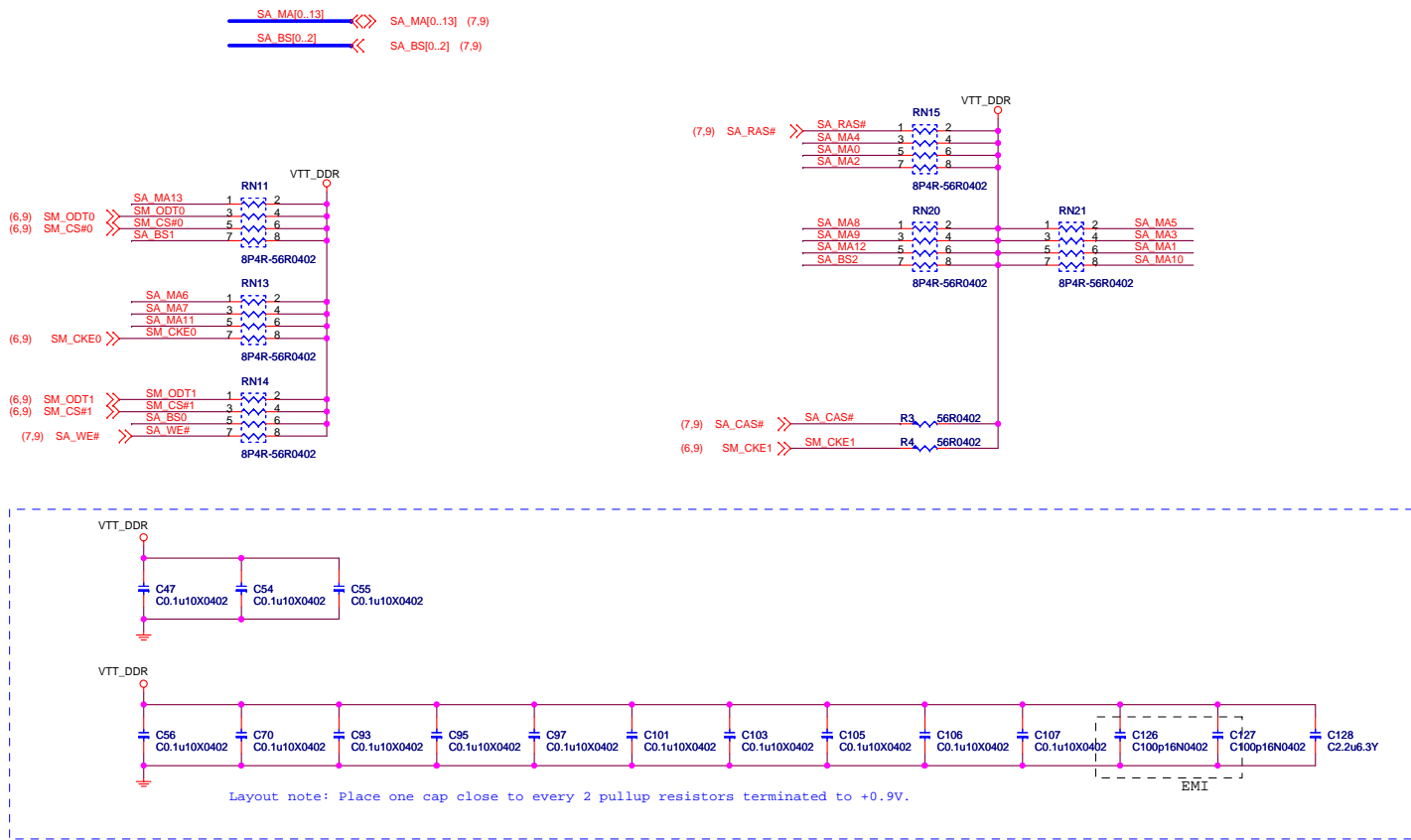






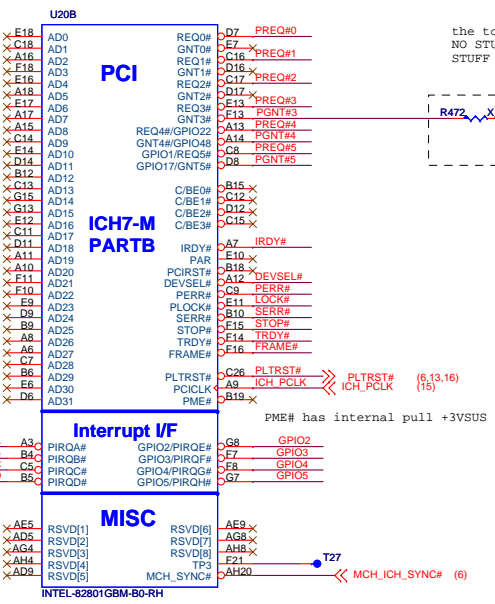
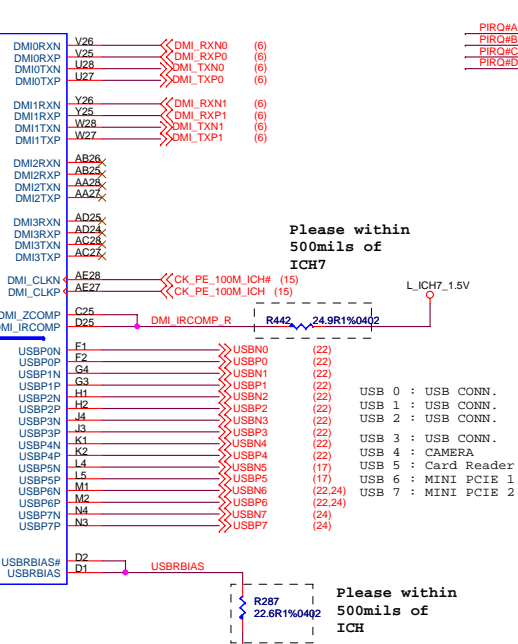
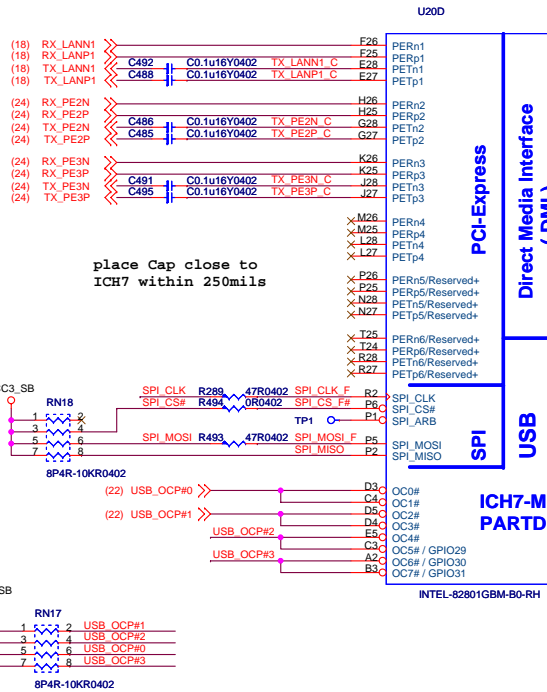
**N13-2000220-A10**  
**Bottom**





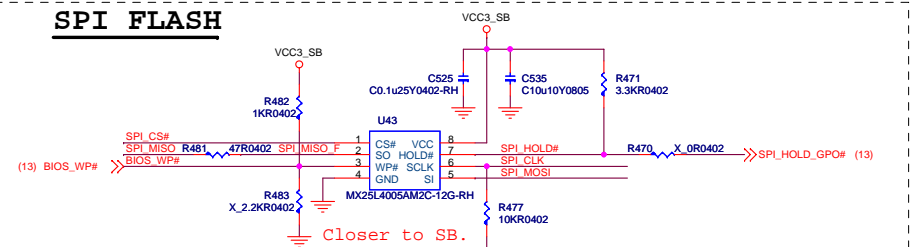
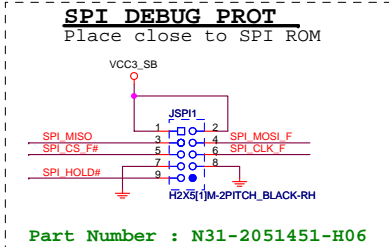
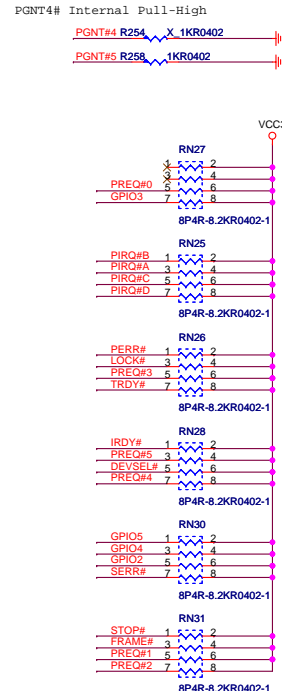
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the top-blisk swap mode  
NO STUFF by default.  
STUFF for A16 swap override

GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC

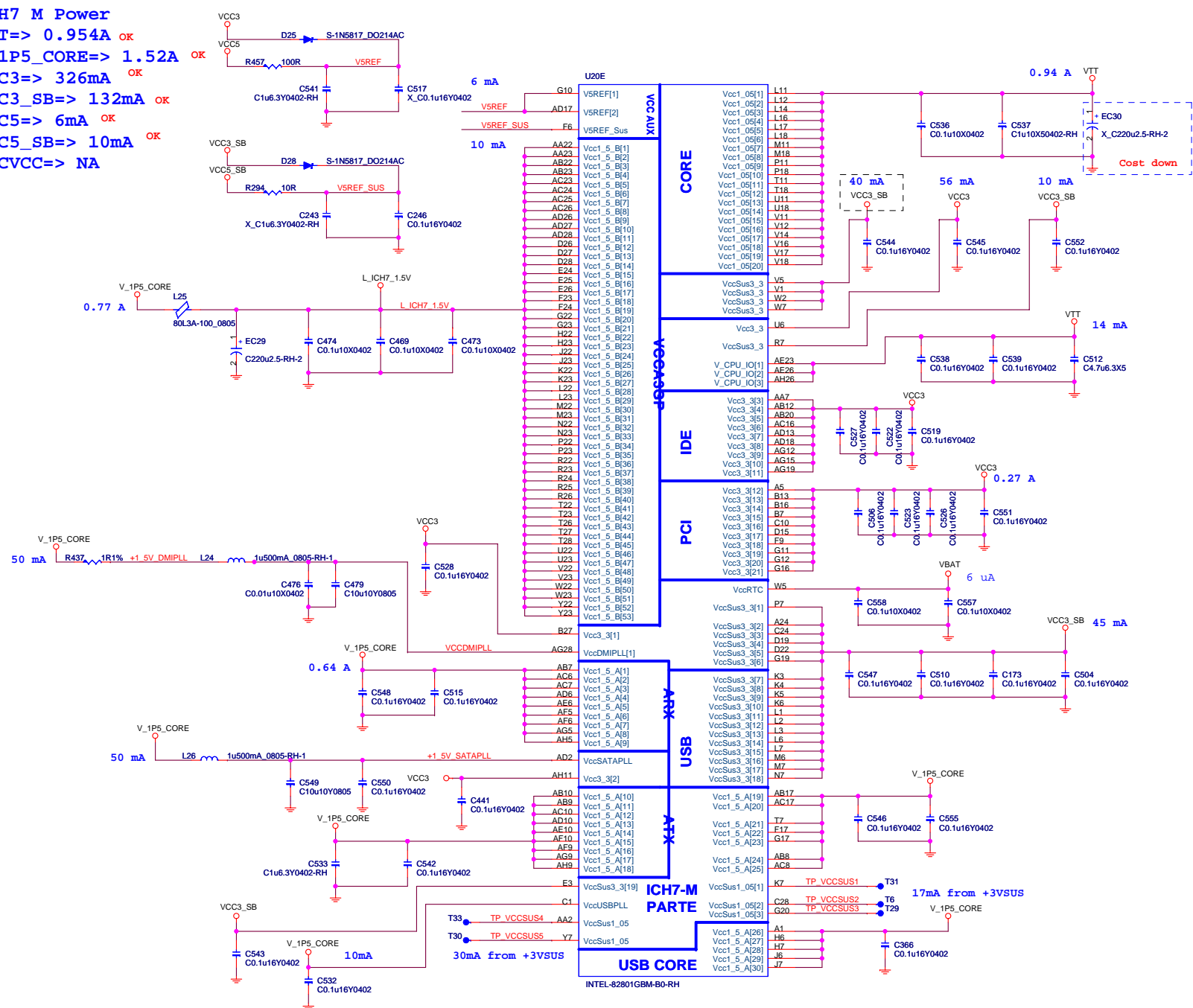




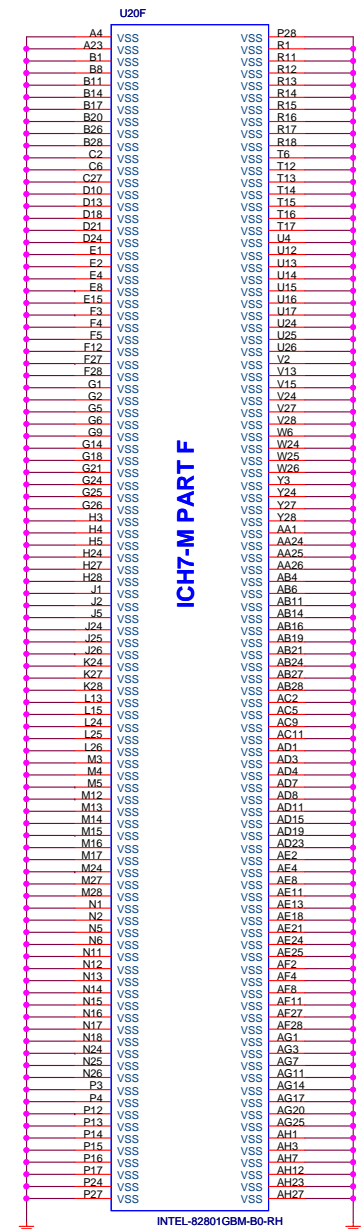
```

ICH7 M Power
VTT=> 0.954A OK
V_1P5_CORE=> 1.52A OK
VCC3=> 326mA OK
VCC3_SB=> 132mA OK
VCC5=> 6mA OK
VCC5_SB=> 10mA OK
RTCVCC=> NA

```



**PIN AA2,Y7,K7,C28,G20 : VccSus 1.05V for RTCVCC**

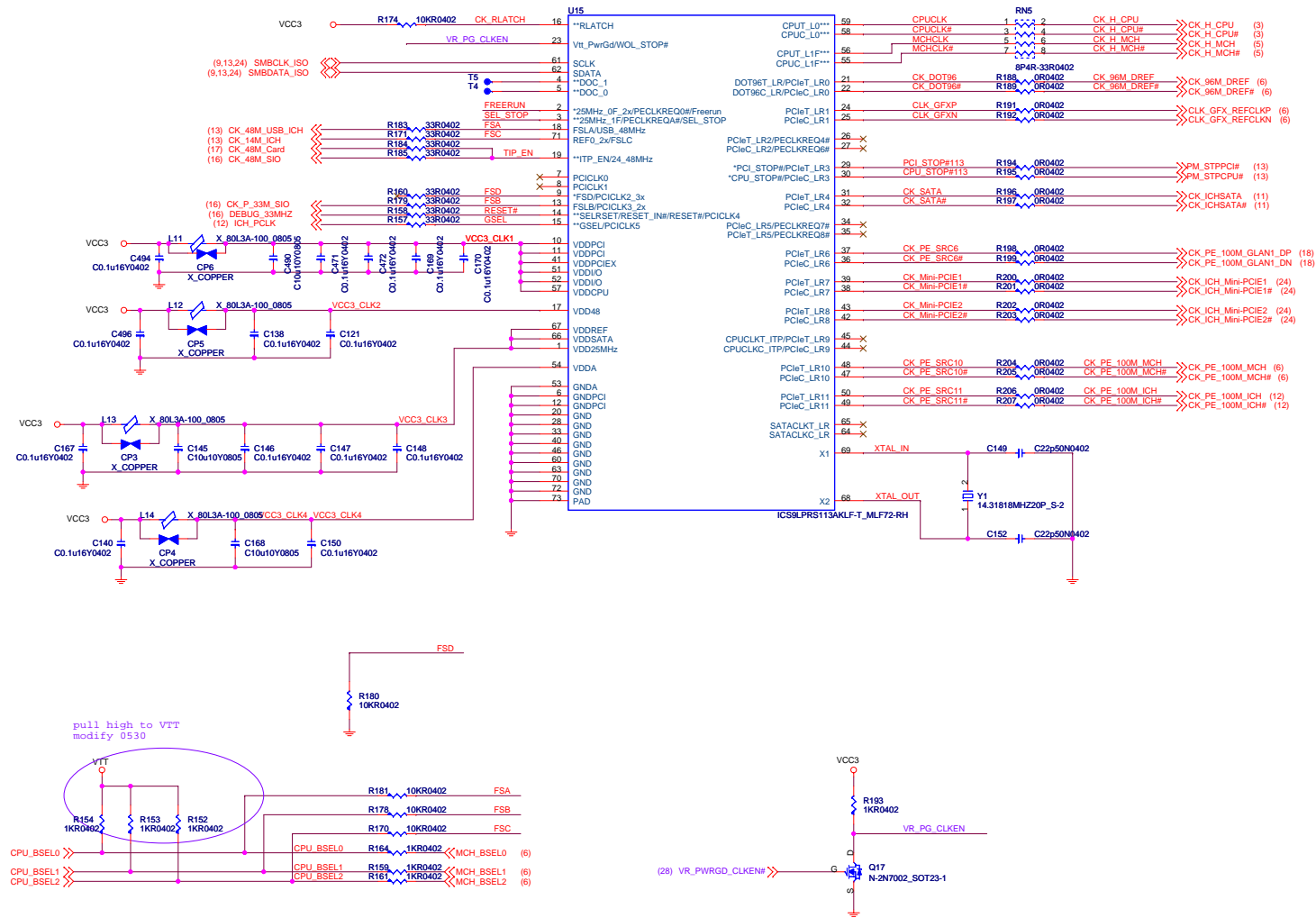


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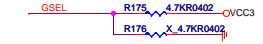
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### CLOCK GEN STRAPING



1 => Pin21/22 96MHz  
0 => Pin21/22 100MHz



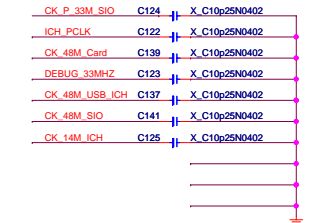
L:PCICLK4  
H:RESET\*  
to be WDT rest=> HI



```
113
TIP_EN=0 => PCIEX9,
TIP_EN=1 => CPU_ITP
```



```
Selects pin 29/830
1 = PCI_STOP#/CPU_STOP#
0 =PCIEX CLK output
```



CPU Table

BSEL[2]	BSEL[1]	BSEL[0]	BCLK
L	L	L	100MHZ
L	L	H	133MHZ
L	H	L	RESERVED
L	H	H	166MHZ

CLK Gen 113

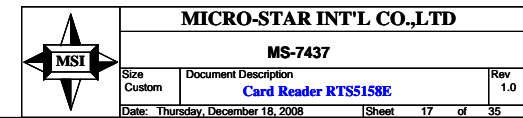
BSEL[2]	BSEL[1]	BSEL[0]	BCLK
H	L	H	100MHZ
L	L	H	133MHZ
L	H	L	200MHz
L	H	H	166MHZ







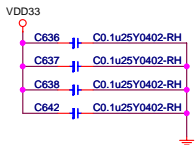
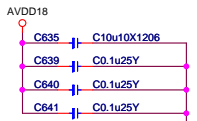
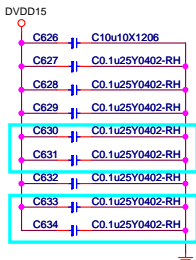
## Flash Card Socket



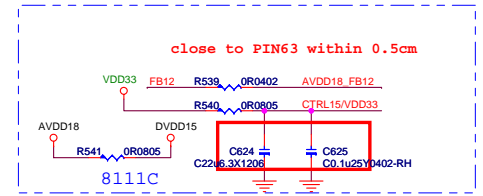
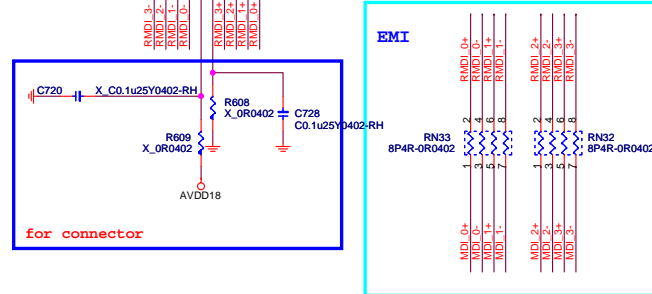
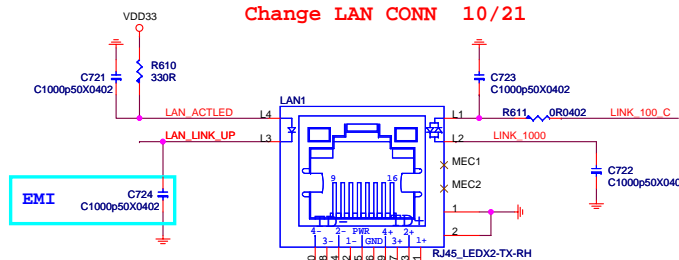
layout close to PIN64

### Power domain chart

	RTL8111C
AVDD33	3.3V
AVDD18	1.2V
EVDD18	1.2V
DVDD15	1.2V

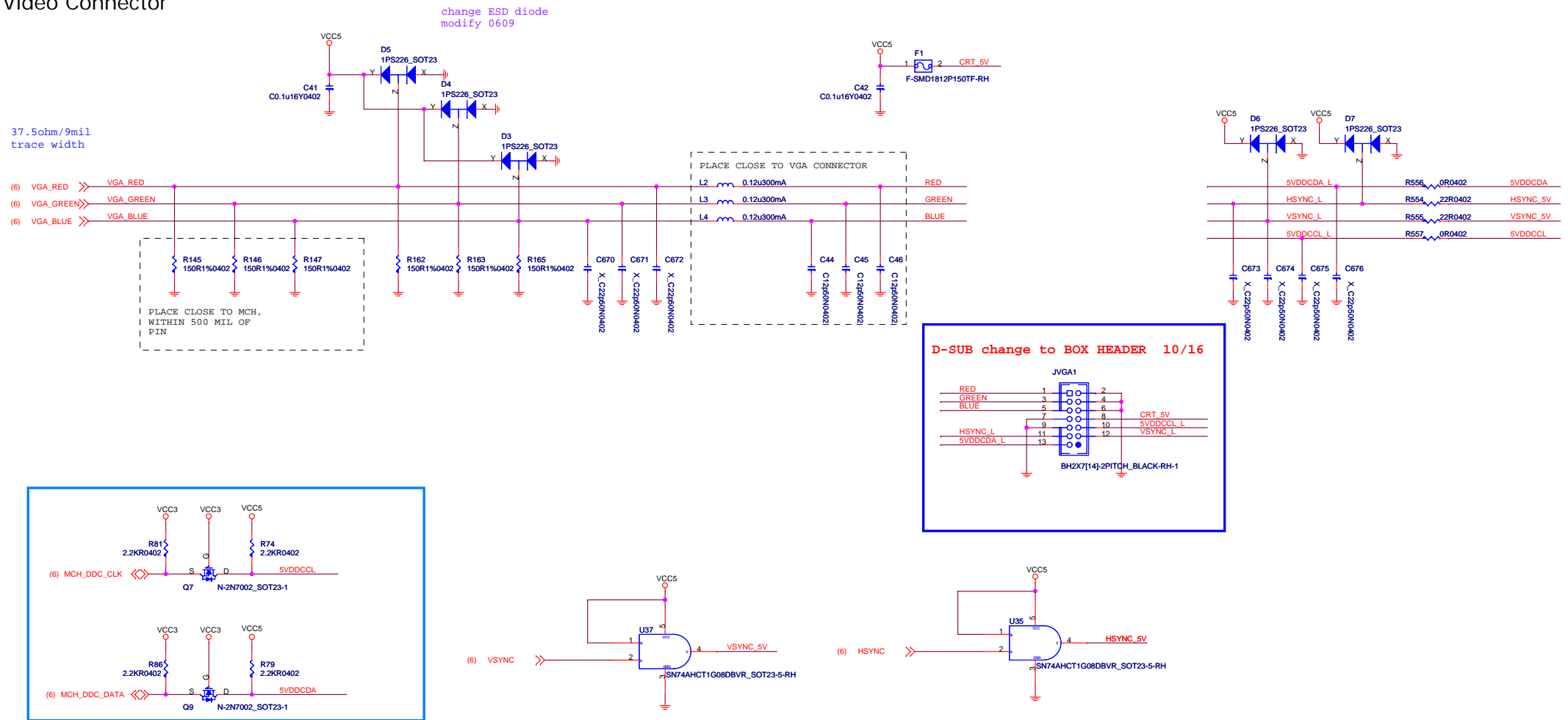


### Change LAN CONN 10/21



Power consumption			
	1G	100M	
3.3V	103mA	TBD	
1.5V	367mA	TBD	
1.8V	198mA	TBD	

## Video Connector





The diagram shows two SATA controllers, SATA1 and SATA2, connected to a common SATA7PM\_ORANGE-P power source. Each controller has four signal lines (RX, RX#, TX#, TX) and a ground connection. The connections are as follows:

SATA Controller	Signal	Capacitor	Component Value
SATA1	SATA_RX0	C262	0.01uF 16X0402
	SATA_RX#0	C261	0.01uF 16X0402
	SATA_TX#0	C260	0.01uF 16X0402
	SATA_TX0	C259	0.01uF 16X0402
SATA2	SATA_RX1	C263	0.01uF 16X0402
	SATA_RX#1	C265	0.01uF 16X0402
	SATA_TX#1	C267	0.01uF 16X0402
	SATA_TX1	C268	0.01uF 16X0402

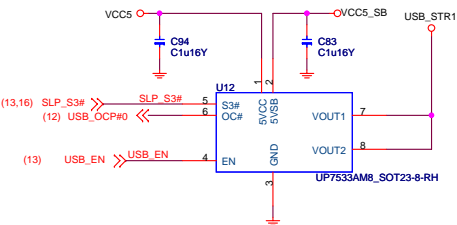
The schematic shows the power plane connections for the JPWR1 connector. VCC5 is connected to pin 1, and VCC6 is connected to pin 2. Both pins are bypassed to ground with capacitors C172, C166, C180, and C186. The capacitors are labeled with their values: C0.1u1S70402 and C10u1070305.

[illegible][illegible]

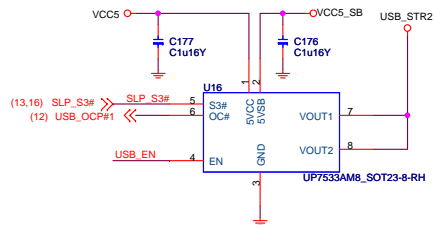
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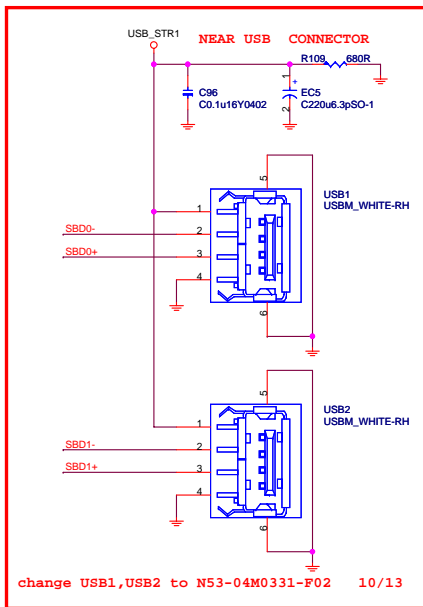
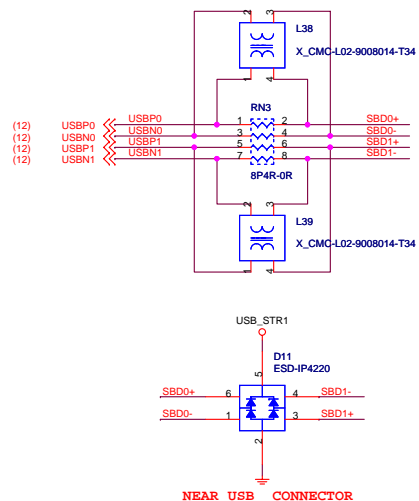
## POWER CIRCUIT FOR USB PORT 0,1



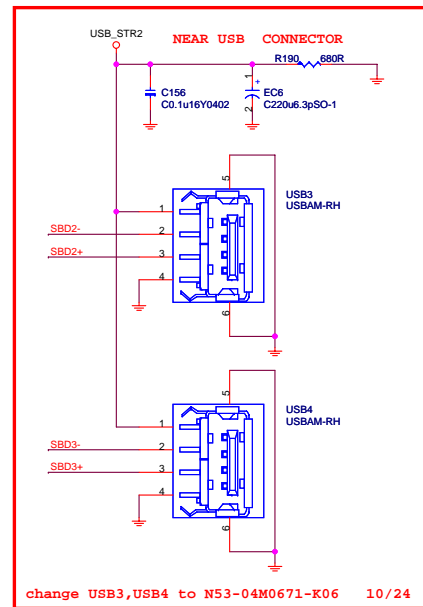
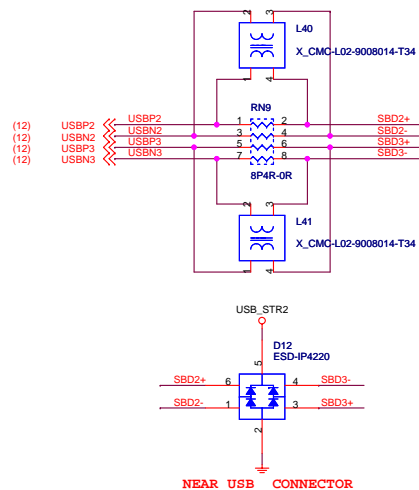
## POWER CIRCUIT FOR USB PORT 2,3



## USB CONNECTOR FOR USB PORT 0,1

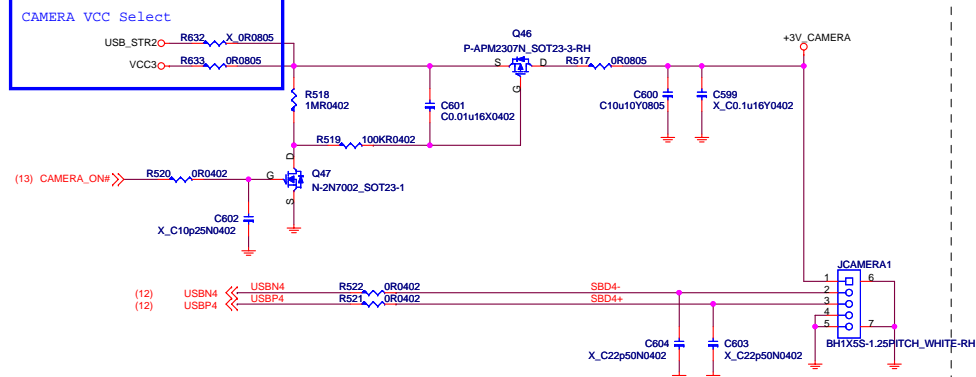


## REAR PANEL USB CONNECTOR FOR USB PORT 2,3

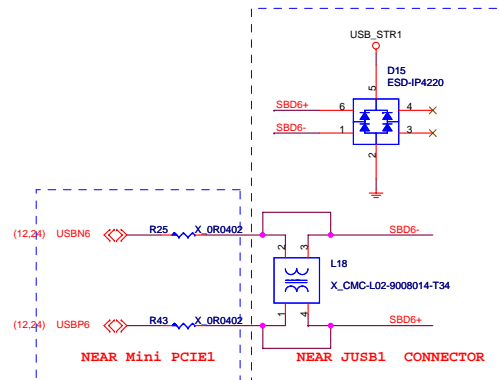


## CAMERA

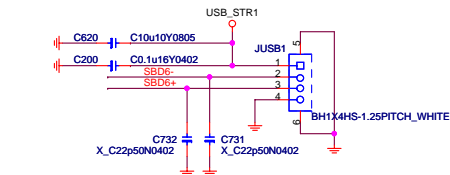
AOC & Channel VCC3  
ViewSonic VCC5 (USB\_STR2)



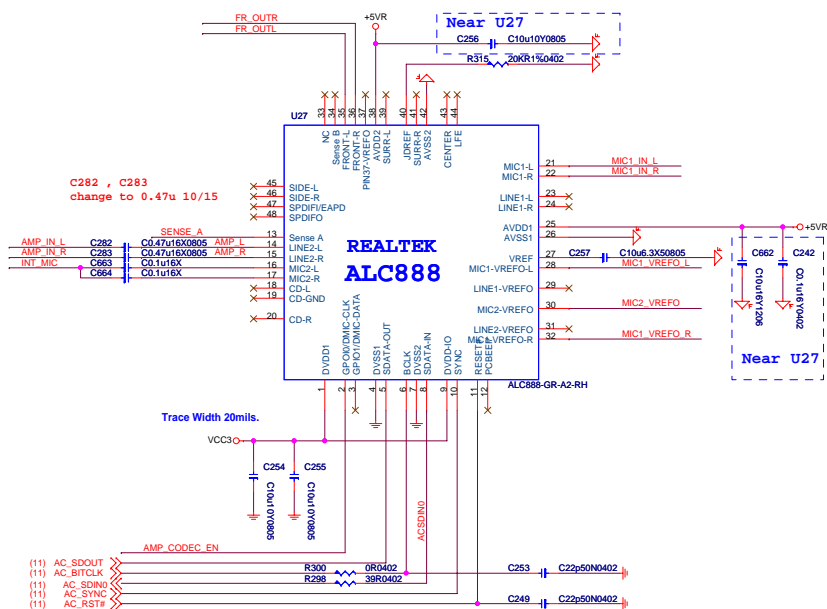
## Touch Panel USB HEADER



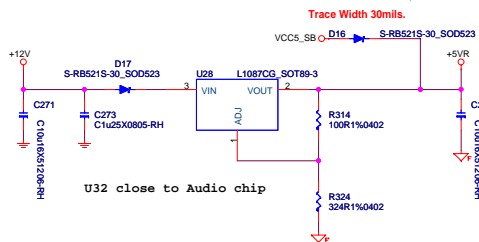
BOM Option Remove R25,R43 for Mini PCIE 1



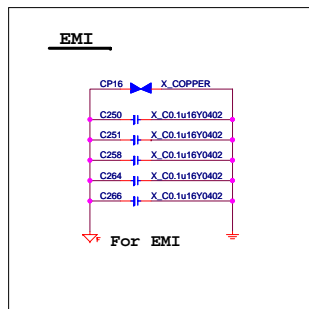
## ALC888 CODEC



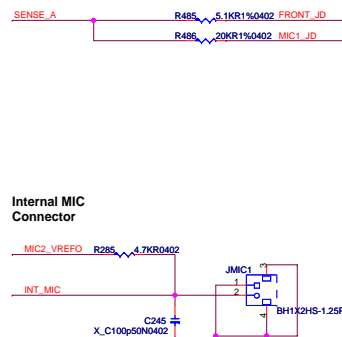
## AUDIO CODE REGULATORS



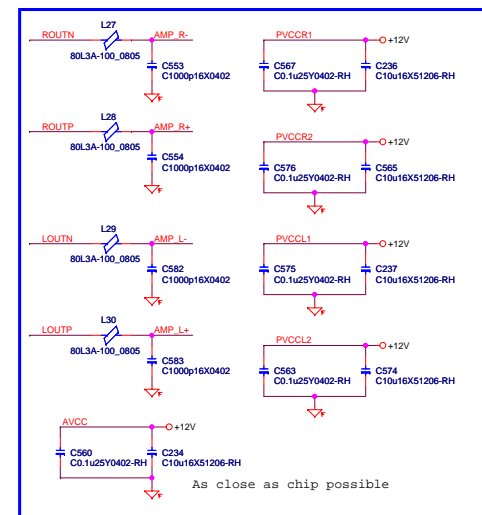
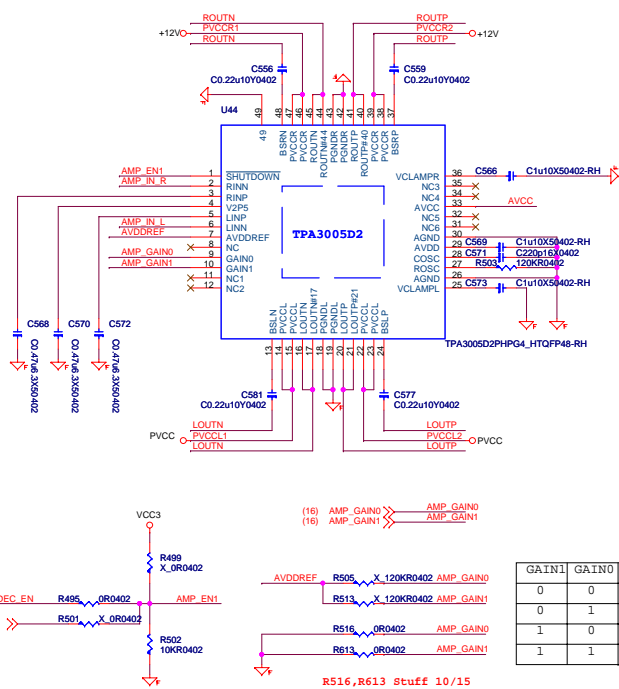
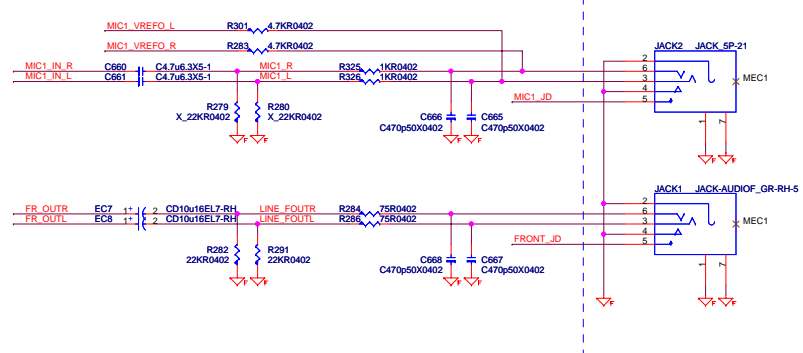
## EMI



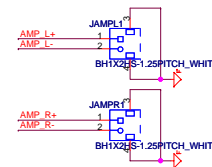
ALC888 JACK DETECT



ALC888 JACK



GAIN1	GAIN0	AV (dB)
0	0	15.3
0	1	21.2
1	0	27.2
1	1	31.8



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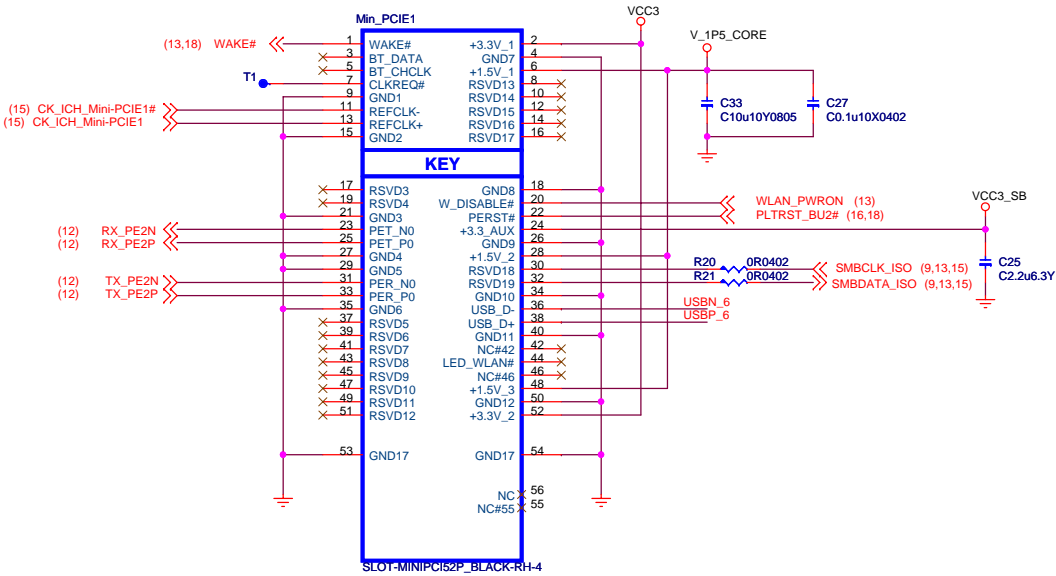
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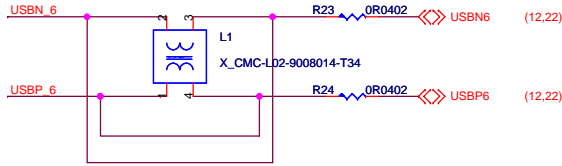
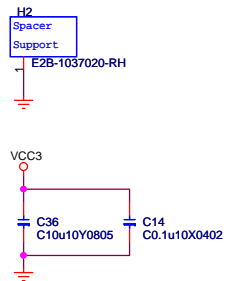
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Mini PCI-E Slot 1

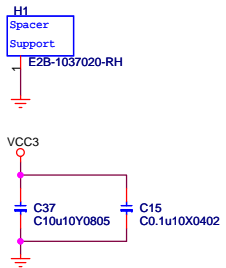
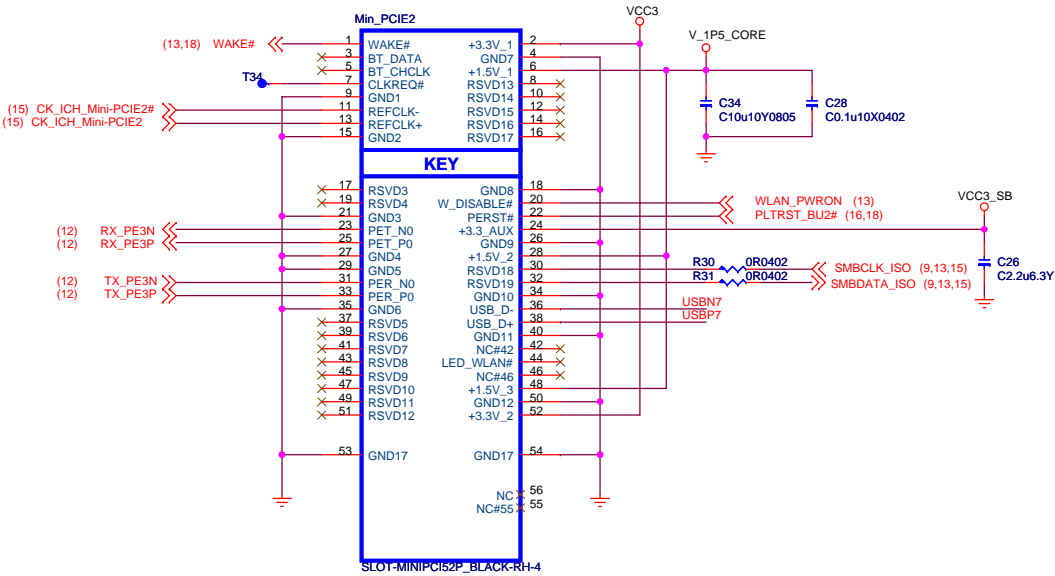
BOM Option Remove for AOC



BOM Option Remove R23,R24 for Touch Panel



Mini PCI-E Slot 2



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**INTEL/PB Front Panel Connector**

Diagram illustrating the internal wiring of the INTEL/PB Front Panel Connector, showing connections to various components and headers.

**Components and Connections:**

- Headers and Connectors:**
  - JFP1:** Header for front panel LEDs and switches. Pins 1-8 are connected to HDD+, HDD\_LED, PWR\_LED, SUS\_LED, and SW1.
  - SW1:** SW-TACTB1-4P\_BROWN-RH switch.
  - SW2:** SW-TACTB1-4P\_S switch.
- Resistors:**
  - R107:** 330R, connected to VCC5 and JFP1 pin 1 (HDD+).
  - R142:** 10KR0402, connected to VCC3\_SB and JFP1 pin 2 (HDD\_LED).
  - R143:** 33R0402, connected to VCC5 and JFP1 pin 3 (PWR\_LED).
  - R150:** 0R0402, connected to FP\_RST# and JFP1 pin 4 (SUS\_LED).
  - R125:** 100R0402, connected to JFP1 pin 5 (SW1) and ground.
  - R128:** 10KR, connected to JFP1 pin 6 (SW2) and ground.
  - R136:** 4.7KR0402, connected to VCC3\_SB and JFP1 pin 7 (SW1).
- Capacitors:**
  - C102:** X\_C0.1u16Y0402, connected to JFP1 pin 1 (HDD+) and ground.
  - C104:** C0.1u16Y0402, connected to JFP1 pin 2 (HDD\_LED) and ground.
  - C108:** C1u10Y0402-RH, connected to JFP1 pin 6 (SW2) and ground.
  - C116:** C1u10Y0402-RH, connected to FP\_RST# and ground.
  - C92:** X\_C0.1u16Y0402, connected to JFP1 pin 7 (SW1) and ground.
- Other Components:**
  - D9:** S-BAT54A\_SOT23, connected to IDEACTP# and ground.
  - VCC5:** Power supply for the SATALED# and IDEACTP# lines.
  - VCC3\_SB:** Power supply for the front panel LEDs and switches.

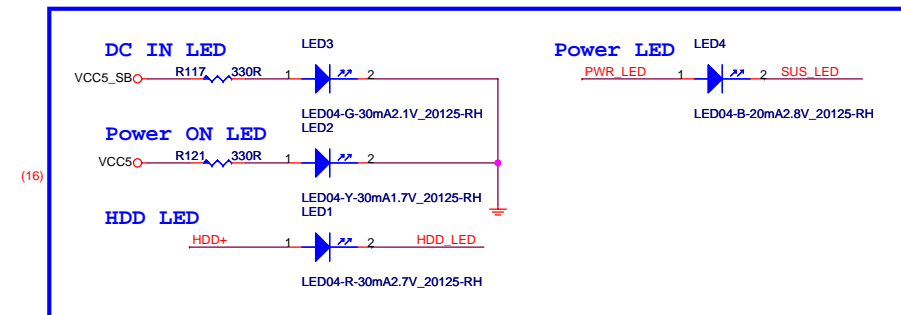
The schematic diagram illustrates the alarm system's output stage. It features three main components: a BEEP input, a SPKR (speaker) output, and a BZ1 (buzzer) output. The BEEP input is connected to a BEEP signal source (represented by a double arrow) and a VCC5 supply. A 4.7K resistor (R299) is connected between VCC5 and the BEEP input. The BEEP input is also connected to a 10K resistor (R296) and the base of an NPN transistor (Q25, NPN-MMBT222A-7-F\_SOT23-RH). The emitter of Q25 is grounded, and the collector is connected to the ALARM output. A red dashed box around Q25 and R296 is labeled "modify 10/13". The SPKR output is connected to a 470R resistor (R297) and the base of another NPN transistor (Q26, NPN-MMBT222A-7-F\_SOT23-RH). The emitter of Q26 is grounded, and the collector is connected to the SPKR output. The BZ1 output is connected to a 470R resistor (R297) and the base of a third NPN transistor (Q26, NPN-MMBT222A-7-F\_SOT23-RH). The emitter of Q26 is grounded, and the collector is connected to the BZ1 output. The BZ1 output is also connected to a VCC5 supply. A red dashed box around Q26 and R297 is labeled "modify 10/13".

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**SYSTEM FAN**

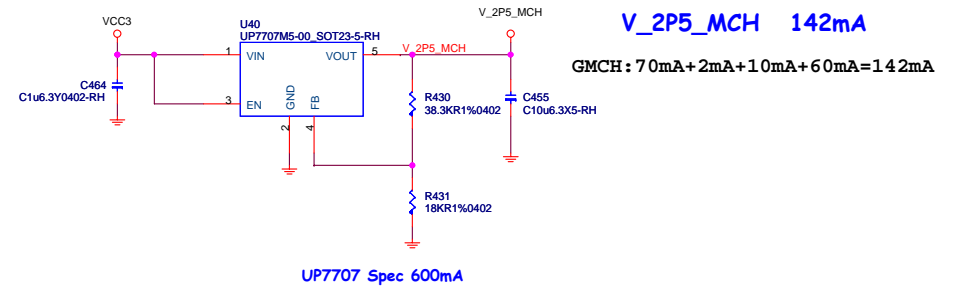
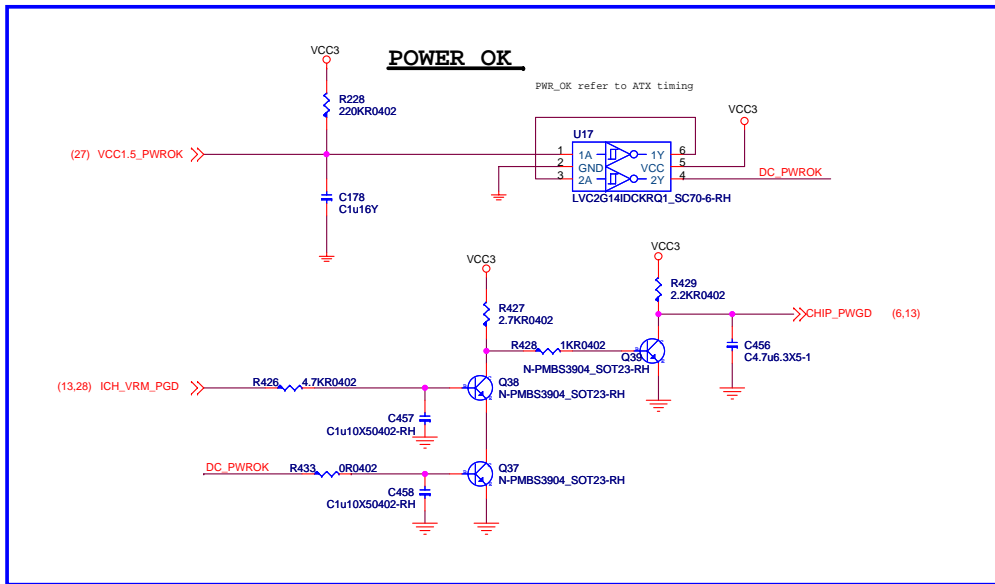
The schematic diagram illustrates the control circuit for the SYSTEM FAN. Key components and connections include:

- Power Supply:** +12V supply connected to the circuit.
- Control Signal:** FAN\_CTL2 (pin 16) is connected to the base of the PNP transistor Q64.
- Transistors:** Q64 (PNP, PMBT3906) and Q63 (NPN, N-2N7002) are used for switching.
- Diodes:** D29 (1N4148W-F), D30 (S-1N5817), and D31 (S-1N5817) are used for protection and signal conditioning.
- Resistors:** R602 (10KR0402), R603 (4.7KR0402), R604 (4.7KR0402), R605 (4.7KR0402), R606 (27KR0402), and R607 (10KR0402) are used for current limiting and signal conditioning.
- Capacitors:** C719 (C10u16X51206-RH), C718 (X\_C10u16Y1206), C717 (C10u16Y1206), C197 (X\_C0.1u16Y0402), C198 (X\_C0.1u16Y0402), and C196 (X\_C0.1u16Y0402) are used for decoupling and timing.
- Relay:** SYS F1 (BHTX3-2.5PITCH\_WHITE-RH-1) is used to control the fan motor.
- EMI Filter:** A dashed blue box labeled 'EMI' contains components C198, C197, C196, and C195.
- Fan Motor:** FANIN2 is the fan motor being controlled.



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## DDR II 1.8V POWER

MAX = 9.2A

VCC\_DDR = 9.02A  
SO-DIMM X1 --- 2.7A  
DDR Terminitor--- 0.6A  
1.5V core --- 4A  
N.B --- 1.72A

MAX = 7.5A

VTT +/-1.05Vcore  
7.174A

Current Limit at 10A  
Current MAX at 8A

CPU Vccp: 2500mA  
GMCH core:2940mA  
GMCH Vccp:780mA  
ICH7M core:940mA  
ICH7M Vcc\_IO:14mA

### DDR VTT Power

To CPU Copper trace width > 250mils , Fill  
island behind DIMM > 400mils .

VTT\_DDR  
1.2A

V\_1P5\_CORE  
4.78A

CPU Vccp: 130mA  
GMCH core:2130mA  
ICH7M core:1520mA  
MINI PCIE :1000mA

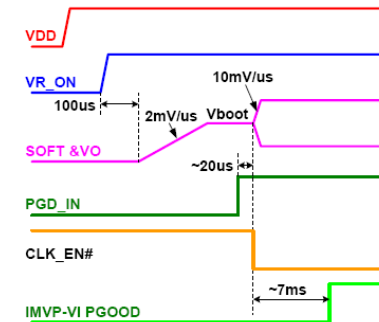
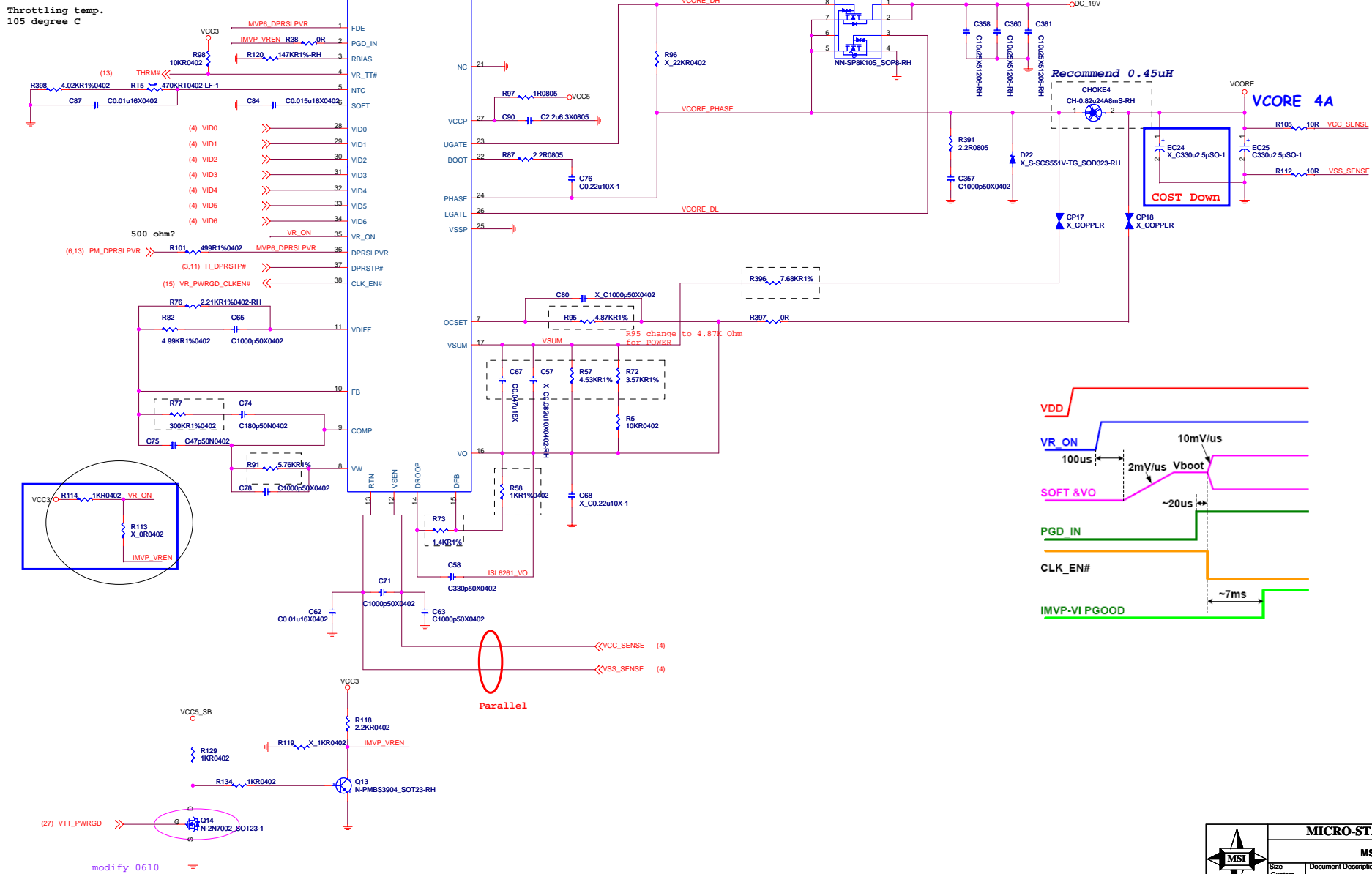
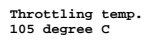
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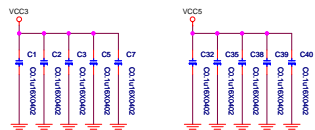
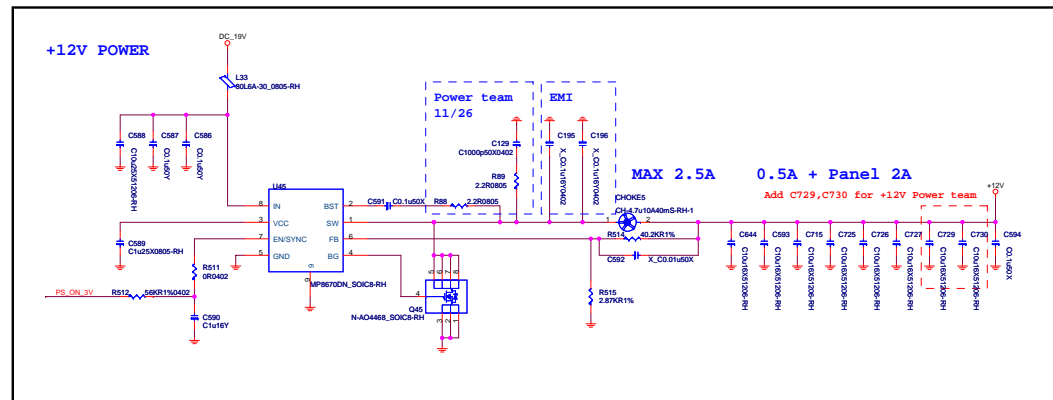
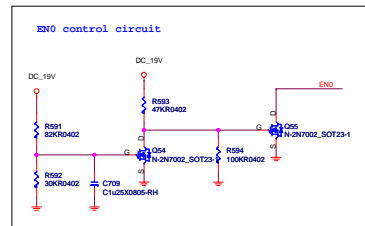
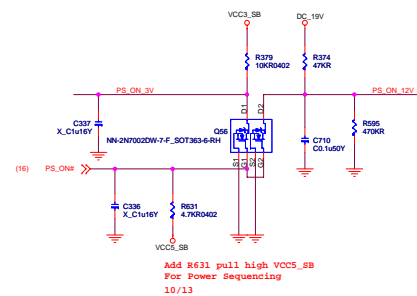
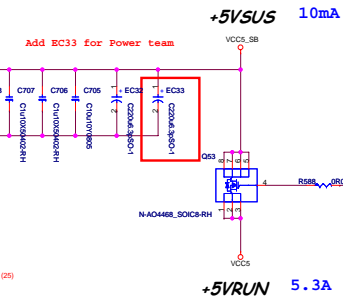
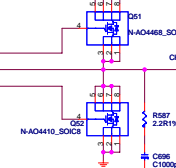
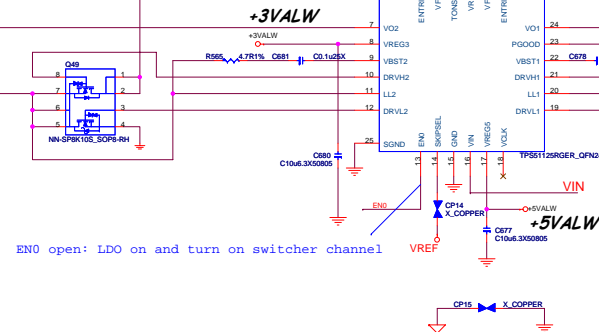
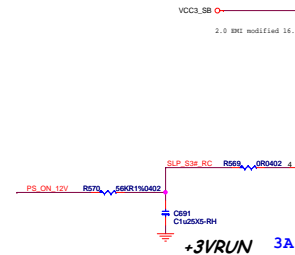
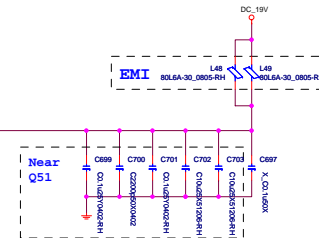
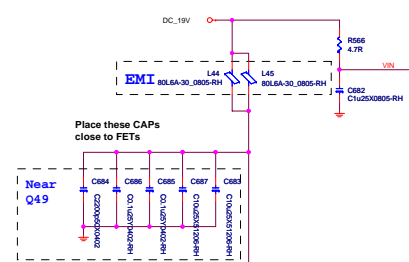


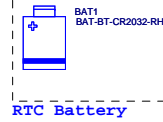
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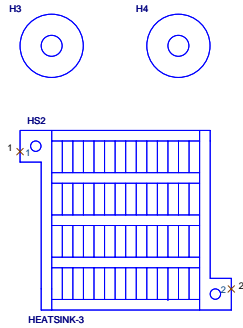
Size	Document Description	Rev
Custom	GMCH VCORE	1.0
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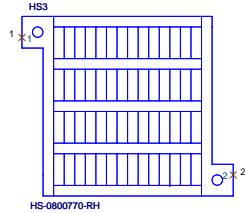




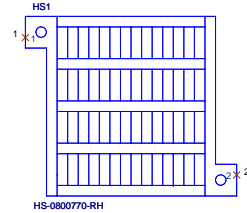
### NB HEATSINK



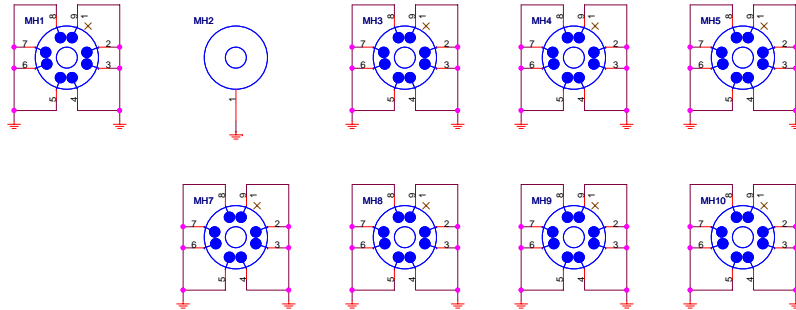
### CPU HEATSINK



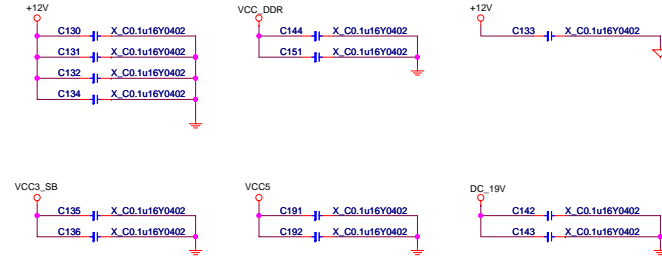
### SB HEATSINK



### Mounting Holes



### EMI

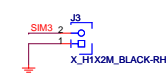


### Simulation

Layer1 / 5mil / 55ohm



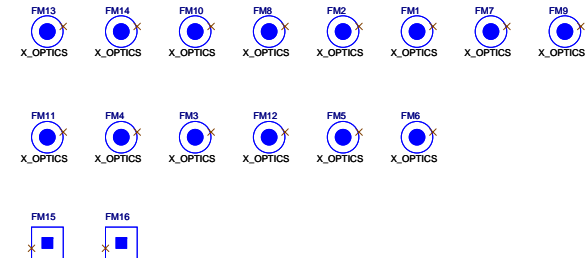
Layer6 / 5mil / 55ohm



Layer4 / 4.5mil / 55ohm



### Optics Orientation Holes



ICH7M


GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Rickles Signal Name
GPIO[0]	BM_BUSY#	AB18	I	VCC3p3	N	Y	3.3	N/A	PM_BMBUSY#
GPIO[1]	REQ[5]#	C8	I	V5REF	Y	N	5	N/A	PREQ#5
GPIO[2]	PIRQE#	G8	I	V5REF	Y	N	5	N/A	GPIO2
GPIO[3]	PIRQF#	F7	I	V5REF	Y	N	5	N/A	GPIO3
GPIO[4]	PIRQG#	F8	I	V5REF	Y	N	5	N/A	GPIO4
GPIO[5]	PIRQH#	G7	I	V5REF	Y	N	5	N/A	GPIO5
GPIO[6]	unmuxed	AC21	I	Vcc3p3	Y	Y	3.3	N/A	ATADET0
GPIO[7]	unmuxed	AC18	I	Vcc3p3	Y	N	3.3	N/A	SIO_OVT#
GPIO[8]	unmuxed	E21	I	VccSus3p3	Y	Y	3.3	N/A	WLAN_PWRON
GPIO[9]	unmuxed	E20	I	VccSus3p3	Y	N	3.3	N/A	NC
GPIO[10]	unmuxed	A20	I	VccSus3p3	Y	N	3.3	N/A	NC
GPIO[11]	SMBALERT#	B23	I	VccSus3p3	Y	Y	3.3	N/A	SMBALERT#
GPIO[12]	unmuxed	F19	I	VccSus3p3	Y	N	3.3	N/A	SPI_HOLD_GPO#
GPIO[13]	unmuxed	E19	I	VccSus3p3	Y	Y	3.3	N/A	SIO_PME#
GPIO[14]	unmuxed	R4	I	VccSus3p3	Y	Y	3.3		NC
GPIO[15]	unmuxed	E22	I	VccSus3p3	N	N	3.3	1	NC
GPIO[16]	DPRSLPVR	AC22	O	Vcc3p3	N	N	3.3	1	DPRSLPVR
GPIO[17]	GNT[5]#	D8	O	Vcc3p3	N	N	3.3	1	PGNT#5
GPIO[18]	STPPCI#	AC20	O	Vcc3p3	N	N	3.3	1	PM_STPPCI#
GPIO[19]	SATA1GP	AH18	I	Vcc3p3	D	N	3.3	1	SATA1GP
GPIO[20]	STPCPU#	AF21	O	Vcc3p3	N	N	3.3	0	PM_STPCPU#
GPIO[21]	SATA0GP	AF19	I	Vcc3p3	N	N	3.3	0	SATA0GP
GPIO[22]	REQ4#	A13	I	Vcc3p3	N	N	3.3	0	PREQ#4
GPIO[23]	LDRQ1#	AA5	O	Vcc3p3	N	N	3.3		NC
GPIO[24]	unmuxed	B3	O	VccSus3p3	Y	N	3.3	1	BIOS_WP#
GPIO[25]	unmuxed	D20	O	VccSus3p3	N	N	3.3	N/A	CAMERA_ON#
GPIO[26]	unmuxed	A21	O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC#5	C3	I	VccsUS3p3	Y	N	3.3		USB_OCP#2
GPIO[30]	OC#6	A2	I	VccsUS3p3	Y	N	3.3		USB_OCP#3
GPIO[31]	OC#7	B3	I	VccsUS3p3	Y	N	3.3		USB_OCP#3
GPIO[32]	CLKRUN#	AG18	O	Vcc3p3	N	N	3.3	1	CLKRUN#
GPIO[33]	AZ_DOCK_EN#	AC19	O	Vcc3p3	N	N	3.3	1	PRES2
GPIO[34]	AZ_DOCK_RST#	U2	O	Vcc3p3	N	N	3.3	0	PRES3
GPIO[35]	SATACLKREQ#	AD21	O	Vcc3p3	N	N	3.3	0	PRES1
GPIO[36]	SATA2GP	AH19	I	Vcc3p3	N	N	3.3	0	SATA2GP
GPIO[37]	SATA3GP	AE19	I	Vcc3p3	N	N	3.3	0	SATA3GP
GPIO[38]	unmuxed	AD20	I	Vcc3p3	Y	N	3.3	1	NC
GPIO[39]	unmuxed	AE20	I	Vcc3p3	Y	N	3.3	1	NC
GPIO[48]	GNT4#	A14	O	Vcc3p3	N	N	3.3	1	PGNT#4
GPIO[49]	CPUPWRGD	AG24	OD	V_FSB_VTT	Y	N	3.3	1	CPU_PWRGD

SIO(F71882)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	UNUSED		
GPIO3	UNUSED		
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	UNUSED		
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	AMP_EN	OUTPUT	RESERVED TO ENABLE THE AMPLIFIER
GPIO15	LED_VSB	OUTPUT	OUTPUT FOR PWR LED
GPIO16	LED_VCC	OUTPUT	OUTPUT FOR PWR LED
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT	PCI RESET BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESET BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESET BUFFER3
GPIO23	UNUSED		
GPIO24	UNUSED		
GPIO26	PSIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PSOUT#	OUTPUT	POWER BUTTON BUFFER OUT TO SB
GPIO30	SLP_S3#	INPUT	FROME SOUTHBRIDGE S3#
GPIO31	PS_ON#	OUTPUT	OUTPUT FOR POWER ON
GPIO32	UNUSED		
GPIO33	RSMRST#	OUTPUT	OUTPUT FOR SOUTHRBRIDGE RSMRST#
GPIO40	AMP_GAIN0	OUTPUT	SET AMPLIFIER GAIN
GPIO41	UNUSED		
GPIO42	UNUSED		
GPIO43	AMP_GAIN1	OUTPUT	SET AMPLIFIER GAIN

DDR-II DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	00	SM_CK0/#0 SM_CK1/#1



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Size Custom

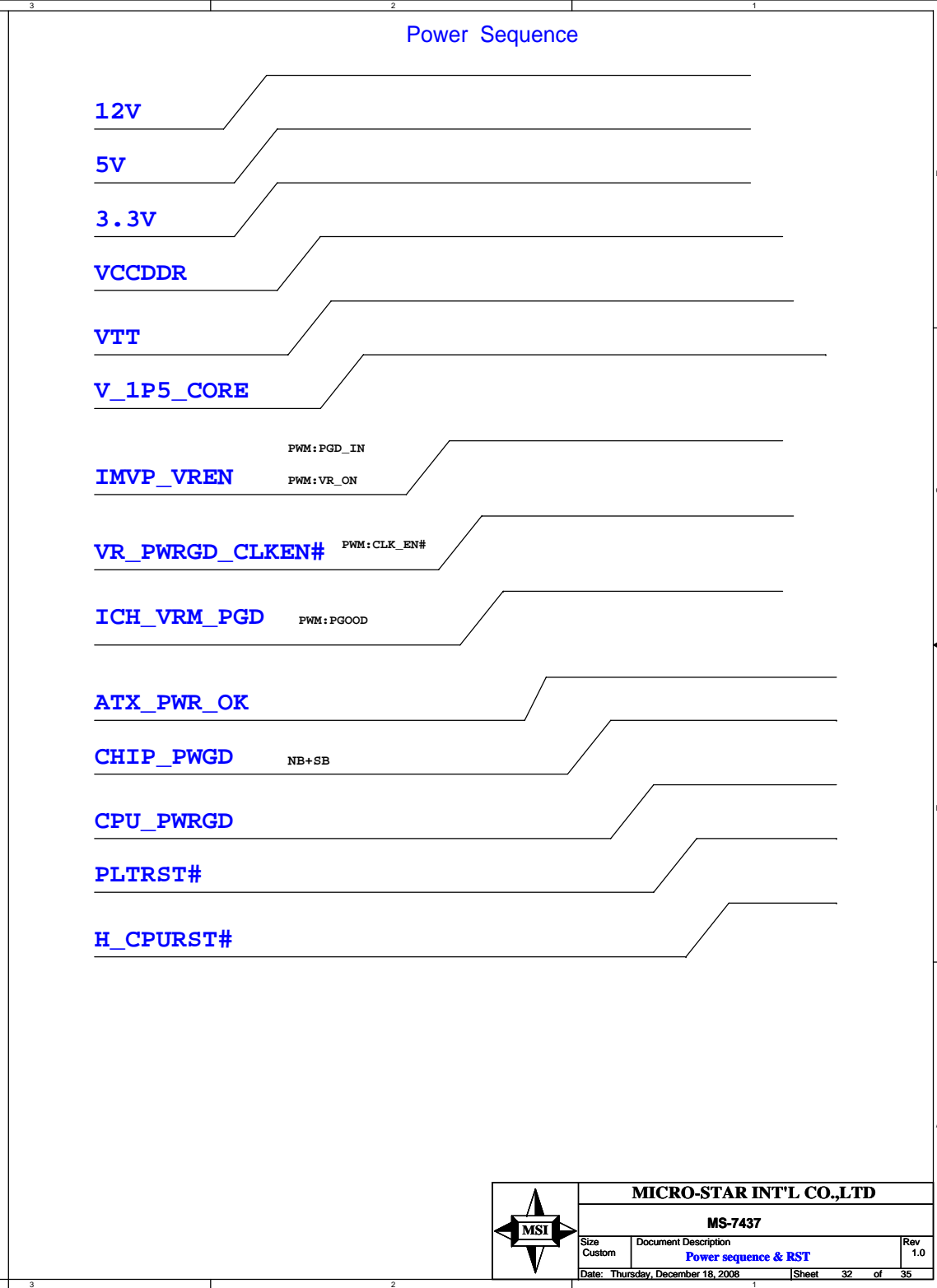
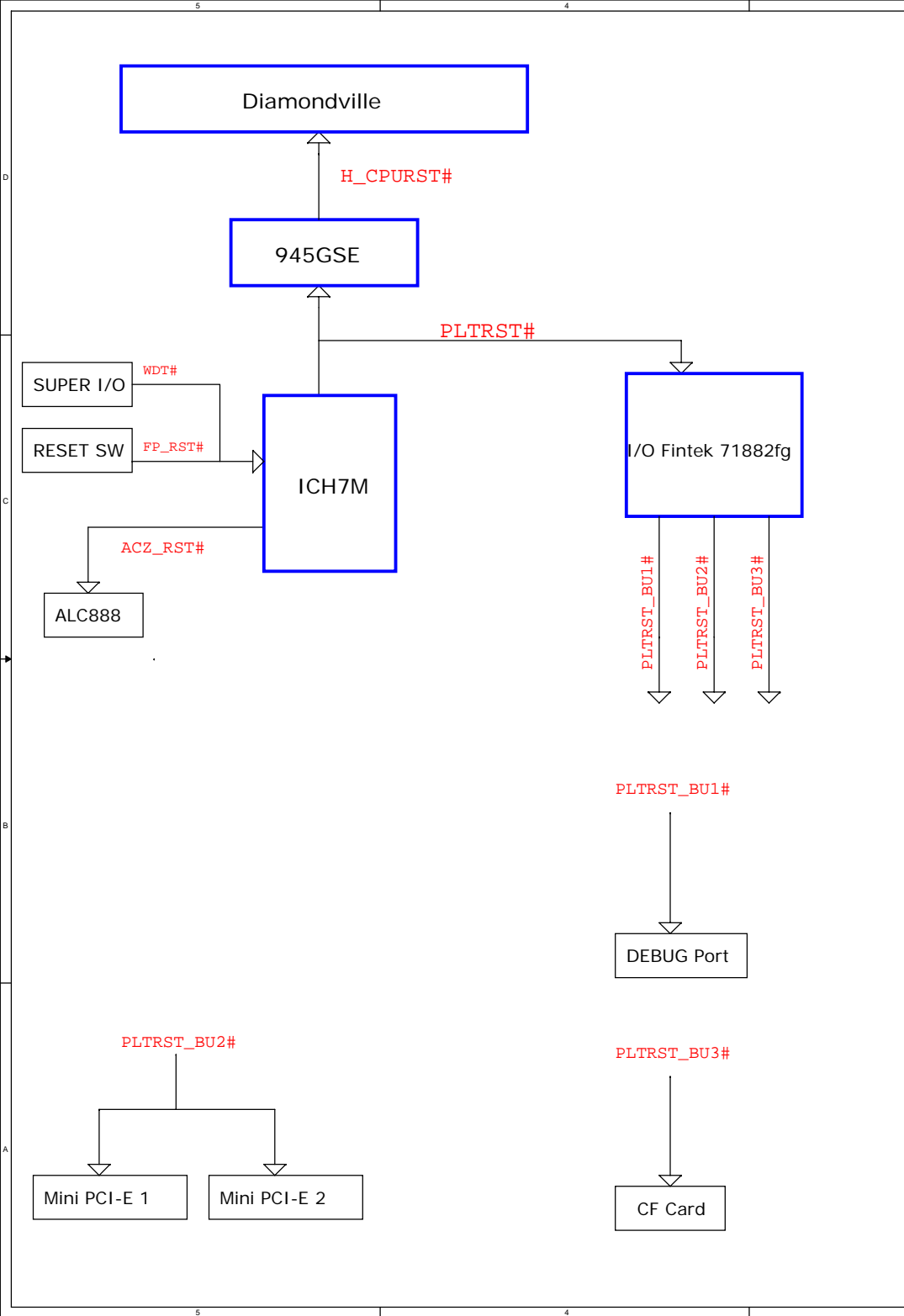
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Rev 1.0

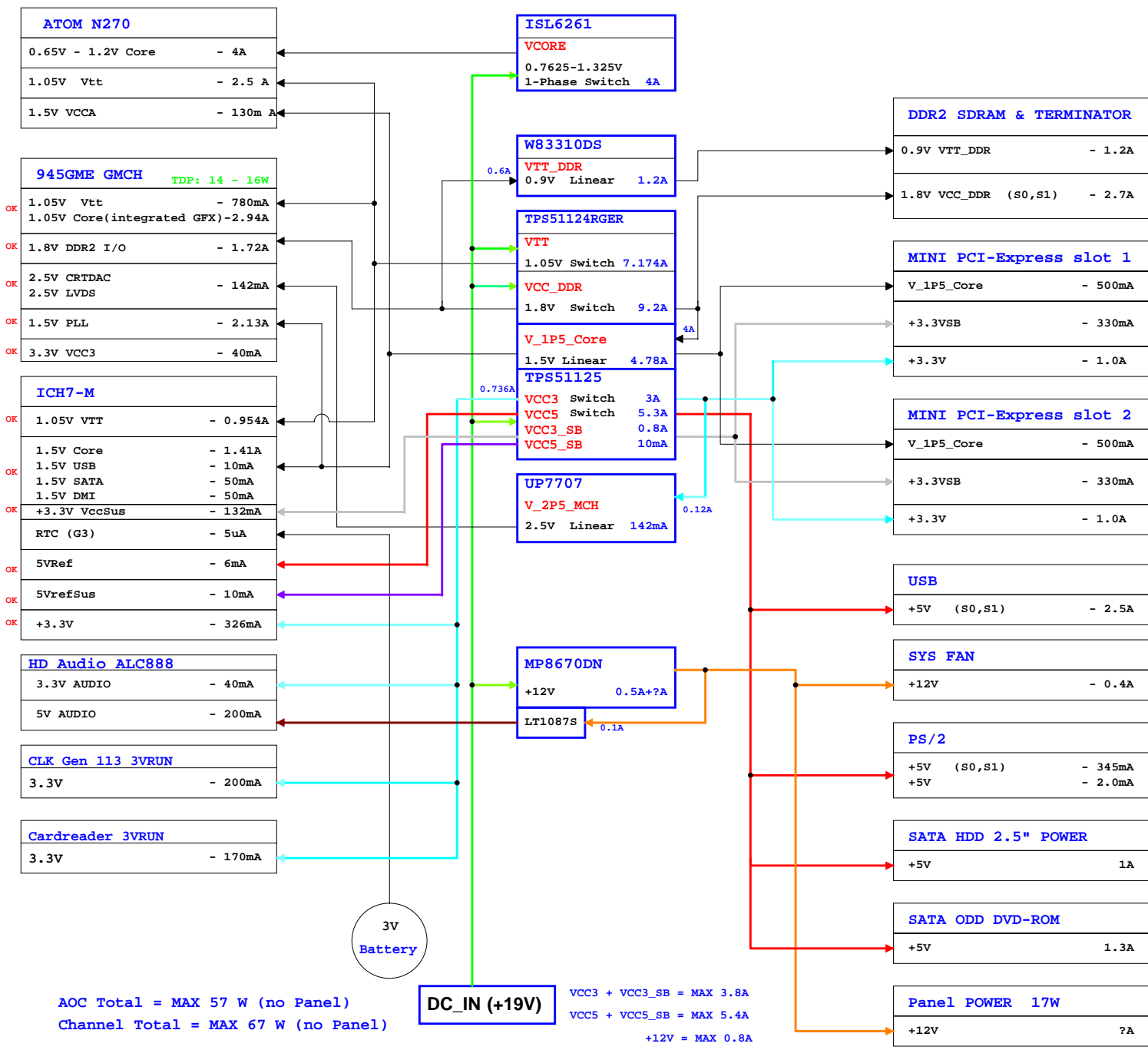
Date: Thursday, December 18, 2008

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**GPIO Setting& PCI Routing**



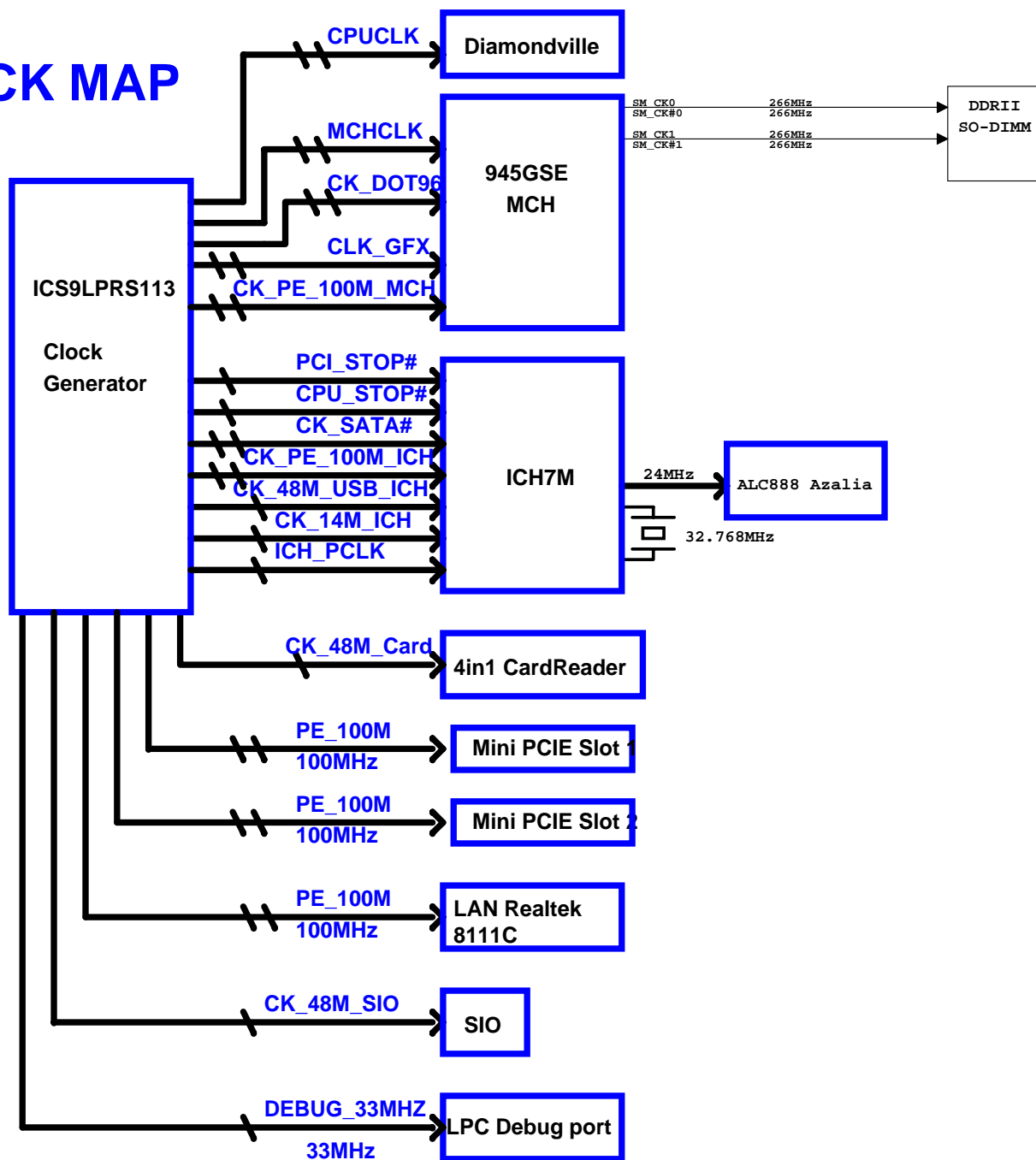




AOC Total = MAX 57 W (no Panel)  
Channel Total = MAX 67 W (no Panel)

VCC3 + VCC3\_SB = MAX 3.8A  
VCC5 + VCC5\_SB = MAX 5.4A  
+12V = MAX 0.8A  
VTT 1.05V = MAX 7.2A  
VCC\_DDR 1.8V = MAX 9.2A

# CLOCK MAP



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1	modify EC21 to 220u/2.5V for Cost	10/6
2	modify EC23 to 220u/2.5V for Cost	10/6
3	modify EC14,EC15,EC16 to 220u/2.5V for Cost	10/6
4	modify EC18 to 220u/2.5V for Cost	10/6
5	modify +3VRun to Vcc3	10/6
6	Add C728 for Lan conn	10/6
7	PS_ON# pull High 4.7K(R631) to VCC5_SB	10/6
8	Add BTB1,C193,C194,R310,SPl for MDC	10/9
9	Add R302~R309 , Remove RN19,C129 for MDC	10/9
10	change USB1,USB2 to N53~04M0331-F02	10/13
11	change R296 to 10K ohm for BUZZER	10/13
12	NO Stuff R346 For Power Sequencing	10/13
13	Add R349 For Power Sequencing	10/13
14	Change PWRJACK1 to N32-1040901-H06	10/15
15	C282 , C283 change to 0.47u for POP Noise	10/15
16	R516,R613 Stuff	10/15
17	D-SUB change to BOX HEADER (JVGA1)	10/16
18	Add EC33 for Power team	10/17
19	Change Jack1,2 P/N for EMI	10/20
20	Change Mini PCIE Slot Main SOURCE to K06	10/20
21	Change LAN CONN	10/21
22	R338 change to 14K Ohm for POWER	10/27
23	R337 change to 9.09K Ohm for POWER	10/27
24	R95 change to 4.87K Ohm for POWER	10/27
25	R560 change to 68.1K Ohm and stuff for POWER	10/27
26	Add C195 , C196 , C197 , C198 for EMI	10/27
27	Add C199 for LAN EMI	10/28
28	Add C729,C730 for +12V (Power team)	10/29
29	NO Stuff EC24 For Cost down	10/31
30	Modify Q64 to 3906 , R603 & R604 to 4.7KOhm for Smart FAN	11/25

[illegible]